REMARKS

In the Final Office Action mailed on June 2, 2006, the Examiner rejected claims 1, 14-15, 18-19 and 43-44 under 35 U.S.C. 103(a) as being obvious over U.S. Patent No. 6,795,841 to Dijkstra in view of U.S. Patent No. 6,889,242 to Sijstermans et al.; rejected claims 20-21 under 35 U.S.C. 103(a) as being obvious over Dijkstra and Sijstermans et al. in further view of the Intel™ IA-32 Architecture Software Developer's Manual; allowed claims 16 and 17 and indicated claims 8-13 as containing allowable subject matter.

In response, Applicant has amended claims 8 and 11 to include the limitations of now cancelled independent claim 1 and cancelled claims 1, 4-7, 14-15, 18-28, 43 and 44. No new matter has been added

Amended claims 8 and 11 are now in condition for allowance. Claims 9, 10, 12 and 13 depend from claims 8 and 11, respectively. Therefore pending claims 8-13, 16 and 17 are in condition for allowance.

In the Final Rejection, Applicant has made several arguments that are incorrect. The Examiner argues in paragraph 8(b) that "the correction factor is already compensated for [by the] rounding error before shifting." The Examiner goes onto to state that "[w]ithout the correction factor" the combination of Dijkstra and Sijstermans et al. would have improved precision over Dijkstra alone. The Examiner is missing the point. The correction factor is allegedly taught by Dijkstra as outlined by the Examiner above. If the combination of Dijkstra and Sijstermans et al. require that the correction factor be removed from Dijkstra, then the proposed combination not only destroys Dijkstra, it also fails to allegedly teach a claimed limitation. Either way, the proposed combination

cannot require a correction factor to "read" on a claim limitation and later remove that correction factor to achieve the desired motivation expressed by the Examiner. Thus, as previously stated by Applicant, the combination of Dijkstra and Sijstermans et al. does not improve the precision of Dijkstra as alleged by the Examiner.

The Examiner also argues that ~(AXORB) is equal to (AXNORB). Applicant agrees but notes the Examiner is again missing point. The question is how many inputs does a bit-wise complement function receive? The claim, before being cancelled, was taking the bit-wise complement of one input. The Examiner cannot read this limitation out of the claim in an effort to make his rejection "fit." Finally, the statement regarding "operat[ing] logic device[s] in [an] untrue state due to power consumption" is a conclusion drawn by the Examiner without any support from a reference. This assumption is also not necessarily true.

CONCLUSION

No fees are believed due for this response. The Office is authorized to charge any needed fees or underpayments of fees (including fees for petitions for extensions of time) under 37 C.F.R. 1.16 and 1.17 to account number 502117. Any overpayments should be credited to the same account.

Applicant respectfully requests reconsideration of the present application, withdrawal of the rejections made in the last Office Action and the issuance of a Notice of Allowance. The Applicant's representative can be reached at the below telephone number if the Examiner has any questions.

Respectfully submitted,

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